**Minutes of meeting : 12th February, 2025**

**Introduction:**

Recap of verification flow

Why is Test plan important?

Electrical Modelling

Which one is more accurate in schematic,layout and Actual device?

Wreal and SVRNM are approximately equally accurate because we cannot model current in them, but on the other side electrical modelling is more accurate than wreal and SVRNM

On what basis do we use SVRNM and wreal modelling?

Who can make decision of deciding whether to use SVRNM or wreal?

**Assignment :**

Continuation of Digital clock

Implementation of digital clock in verilog

**Discussion :**

**Testbench Architecture:**

JTAG: to test and verify the chip

1.Why do we need ports?

Ports of the blocks are generally used for interacting with other blocks.The tb-top.vams

doesn’t have any port names because it does not interact with other blocks , but it consists of

DUT , digital verification environment,and analog pins.

2.What to reuse and how to reuse?

Digital blocks are the one which are reusable.

(If chip is given with 3 analog pins(A1,A2,A3) ans it uses two communication protocols (I2C,JTAG) and it has 3 output which are analogous in nature and asked to verify it)

For verification of digital blocks SV environment is used.

To verify analog blocks we use analog pins.

To monitor the outputs of this chip analog pins are used.

**Analog Pins:**

* To Provide voltage
* To Connect and Disconnect models
* To provide Load

(We can also connect direct schematics instead of models, which can be done with the help of cadence virtuoso)

**Sequence and Sequencer :**

Sequence : It starts or generates the sequence

Sequencer: It drives or controls the sequence

Digital and analog Interface to transfer the signals with each other in verification environment

To use digital verification environment without instantiating it in top module:

We verify the digital blocks separately

To monitor the output current ,Load resistor is required which is connected to the ground.

**Conclusion:**

Discussed question on selection of modelling (wreal or SVRNM)

AMS testbench architecture ;

* Digital Verification Environment
* Analog pins
* Analog and Digital interface